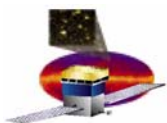


# GLAST Large Area Telescope:

## ACD Integration & Test

Jim La/ACD I&T Lead  
NASA/GSFC/Code 568

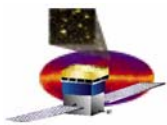
[james.m.la@nasa.gov](mailto:james.m.la@nasa.gov)



# Outline

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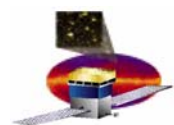
- ☐ **ACD I&T Overview**
- ☐ **I&T Assembly/Integration Flow**
- ☐ **Electrical Interface and Integration**
- ☐ **Performance Verification**
- ☐ **Environmental Testing**
- ☐ **Performance Tests**
- ☐ **I&T Level Communication**
- ☐ **Key I&T Schedule**
- ☐ **Summary**



# ACD I&T Overview

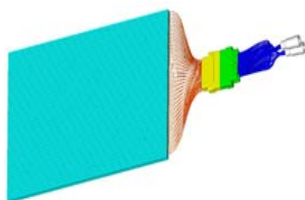
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- ❑ **ACD I&T is the focal point of ACD integration activities**
  - **I&T team plans and manages activities**
  - **ACD team members provide support for integration & test**
- ❑ **Total I&T effort involves all aspects of the ACD – detectors, mechanical, electrical, assembly, performance testing, and environmental testing**
  - **Support ACD/LAT integration and test at SLAC**
  - **Support LAT Environmental Test at NRL**
- ❑ **ACD integration will be in a class 100,000 clean tent at GSFC Building 7/10. Integration area will have sufficient space for electrical works, blanket works, and storage for flight hardware**
- ❑ **GSFC Work Order Authorization (WOA) System will be used**
- ❑ **GSFC Non-Conformance Reporting (NCR) System will be used**
- ❑ **ACD is sensitive to Helium. Helium monitoring is required when the ACD is moved to a new location and then periodic monitoring thereafter**



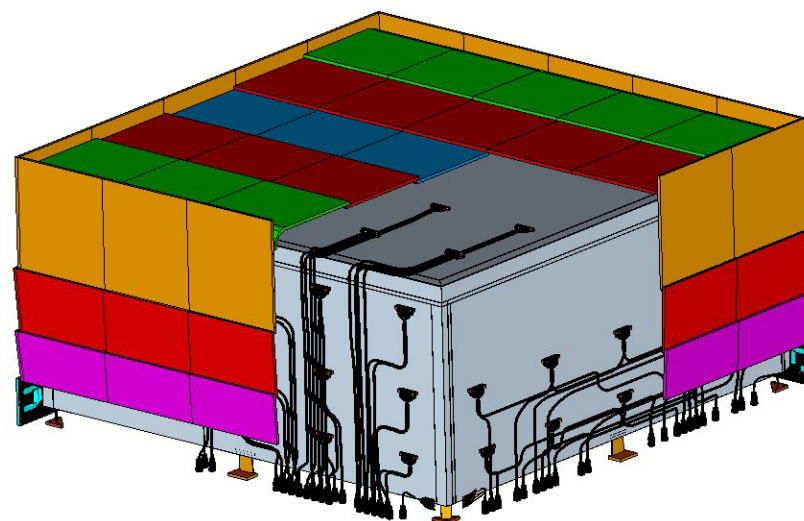
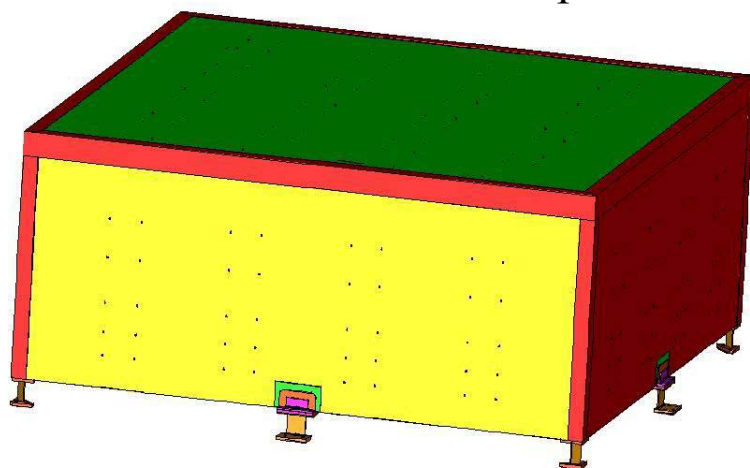
# ACD I&T Overview - Assembly

## Shell, Tile Detector Assemblies (TDA) & Tile Shell Assembly (TSA)

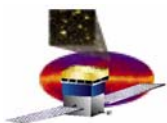


Tile Detector Assembly (89)

Composite Shell

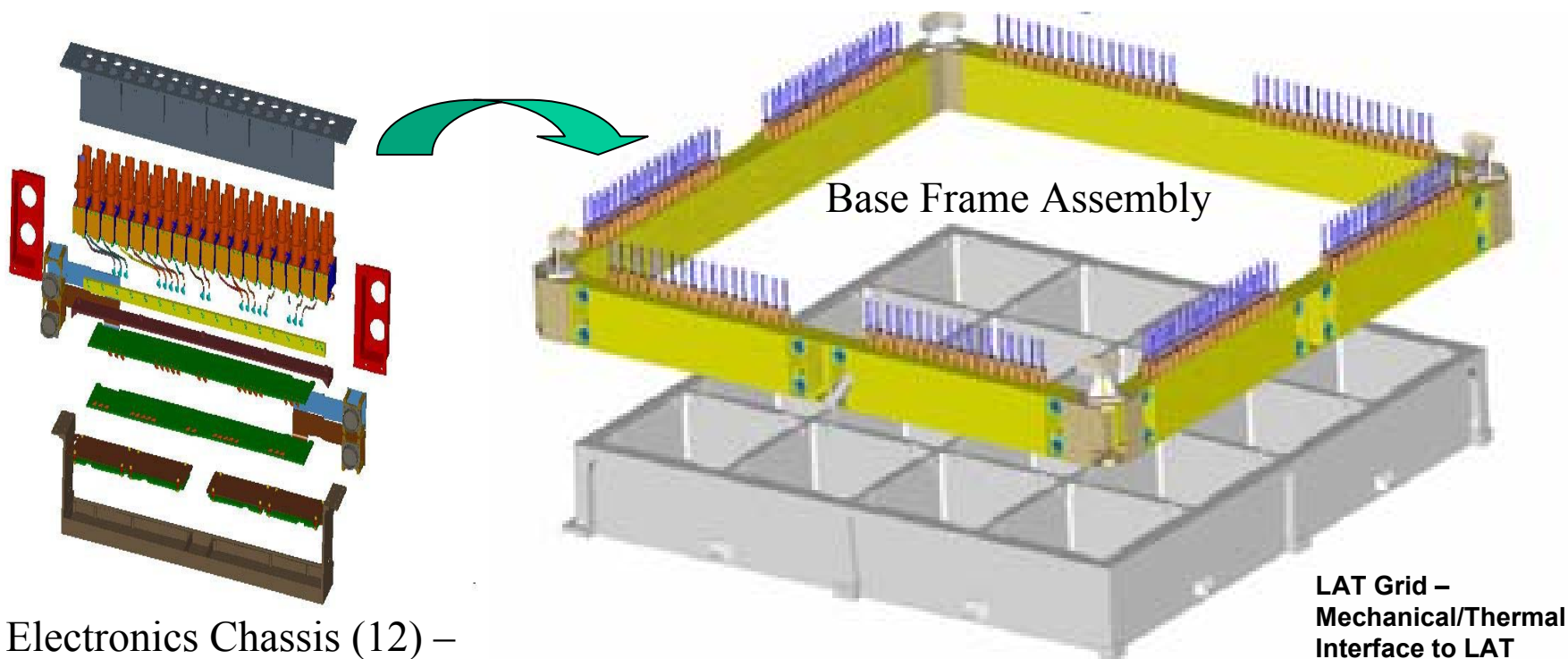


**Mounting the TDAs  
and ribbons on the shell  
forms the TSA**



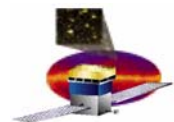
# ACD I&T Overview - Assembly

## Electronics Chassis, Base Frame, and Base Electronics Assembly (BEA)



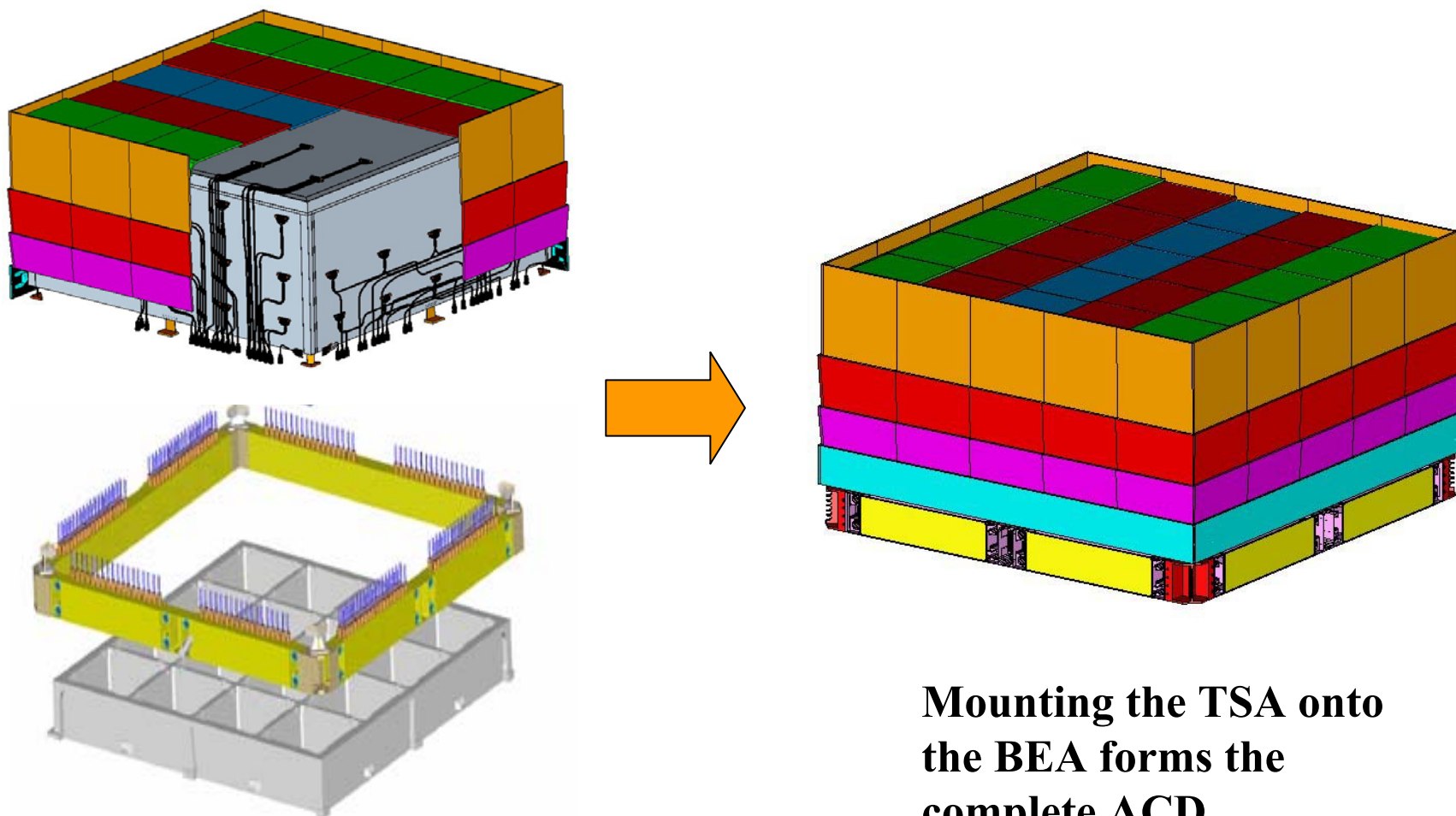
Electronics Chassis (12) –  
Phototubes, FREE Cards,  
HVBS

**Mounting the Electronics Chassis  
into the Base Frame Assembly  
forms the BEA**



# ACD I&T Overview - Assembly

## Tile Shell Assembly (TSA), Base Electronics Assembly (BEA), and ACD

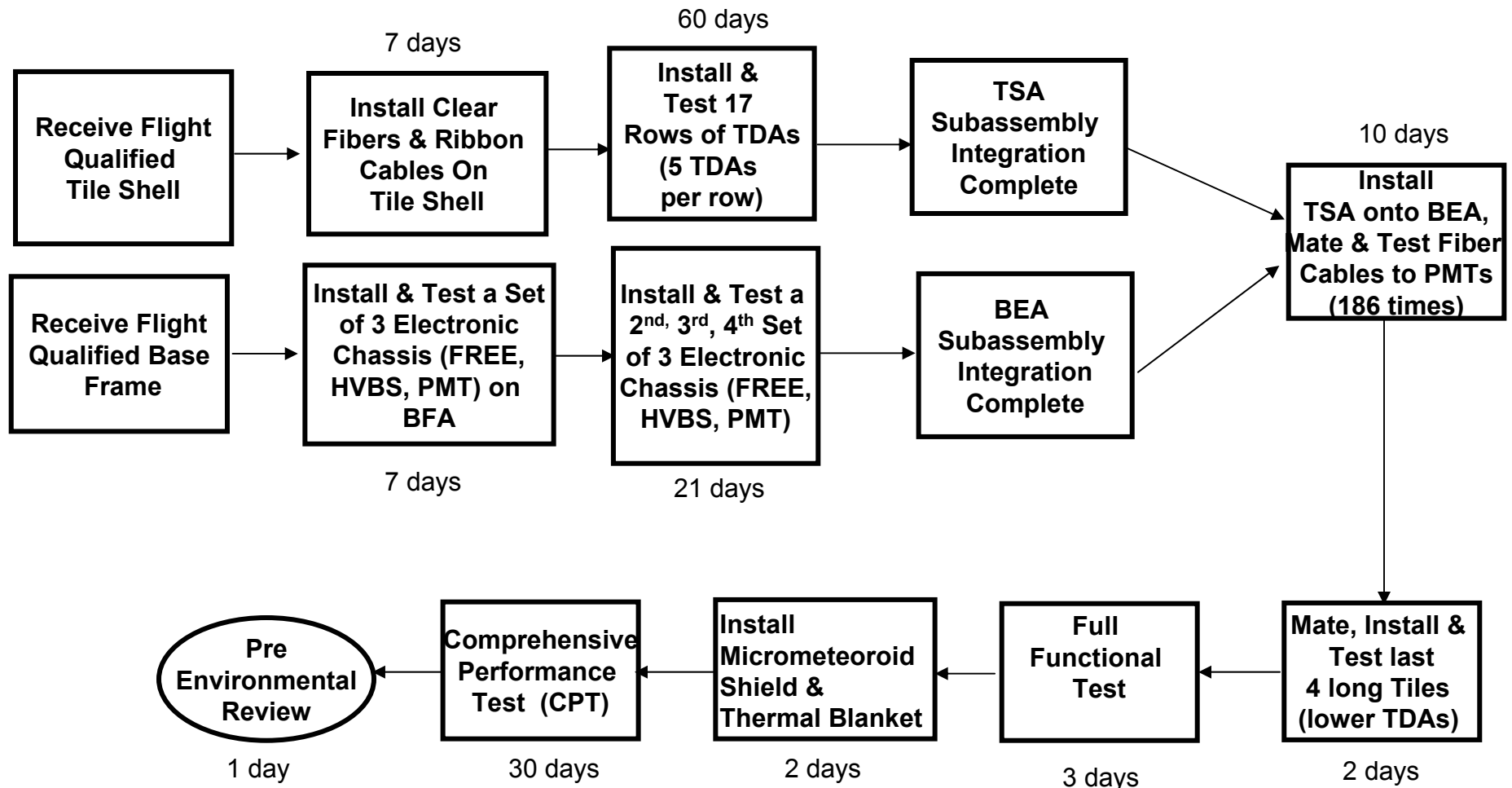


**Mounting the TSA onto the BEA forms the complete ACD**

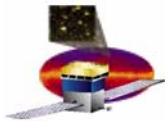


# ACD I&T Assembly/Integration Flow

- Major activities in I&T flow have been defined (LAT-TD-00430-D1)

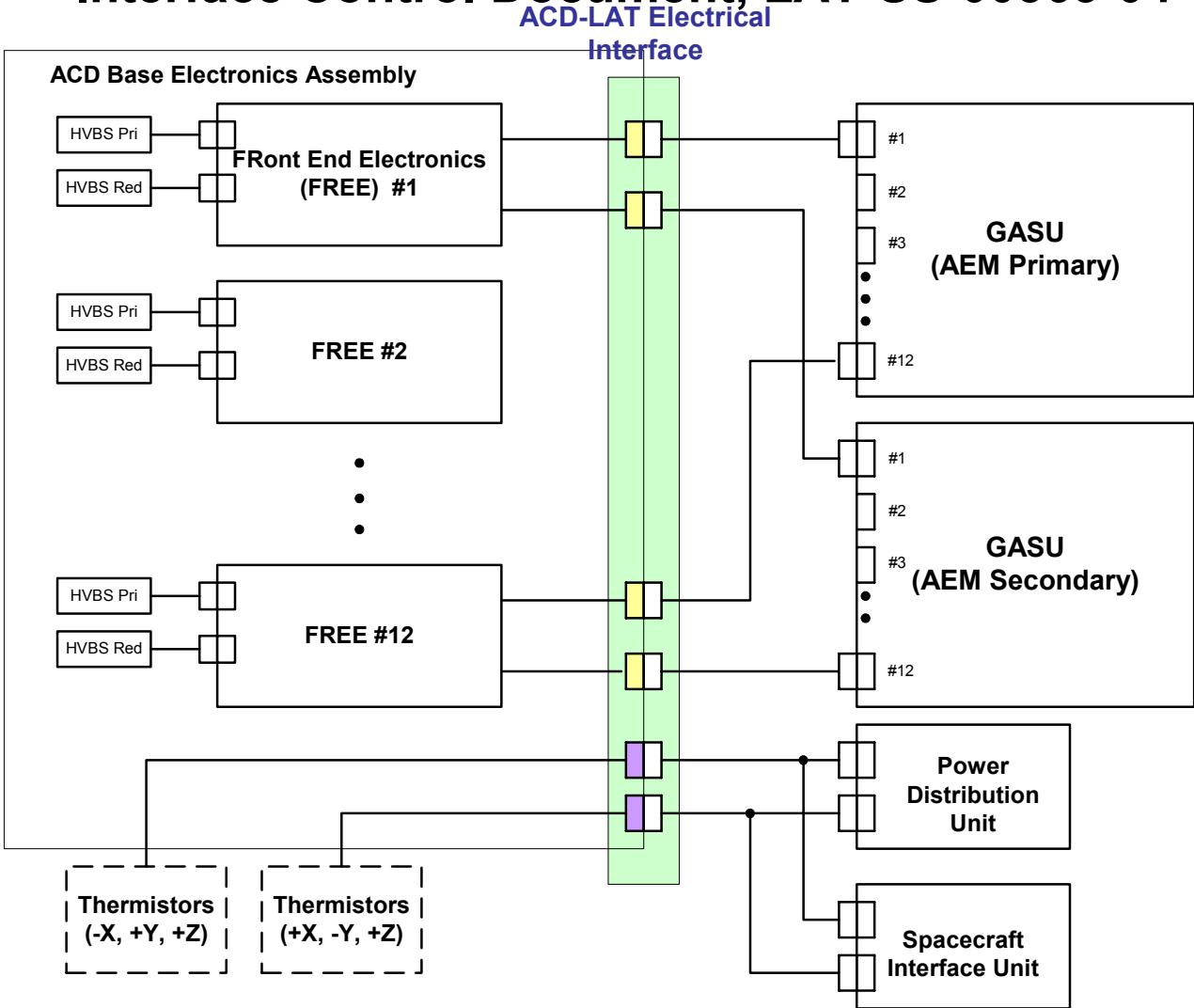




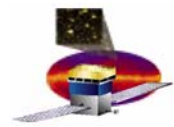


# ACD-LAT Electrical Interface

## Interface Control Document, LAT-SS-00363-04







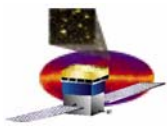
# ACD-LAT Electrical Integration

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**Electrical integration consists of the following for each connector:**

- With all instrument power removed, install connector savers on the component (also on the harness if space allows).
- Install Break-Out Box (BOB), with all jumpers removed, between the component and the harness;
- Perform an isolation/continuity check.
- Supply power to the component and perform an open-circuit voltage check. Remove power from the component.
- If connector supplies power, perform Initial Power Turn-On (IPTO). Remove power from the component.
- Install jumpers, reapply power, and verify connector performance;
- Perform functional test (with BOBs installed)
- Remove all BOBs and re-mate the harness to all the connectors.
- Re-run the functional test.

**Procedures are based on standard Goddard electrical integration approach.**



# Performance Verification Plan

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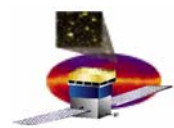
## ACD-PLAN-000050–D5, LAT ACD Subsystem - ACD Verification Plan

### ☐ Purpose and Scope

- Provide means to verify ACD Performance, Functional & Environmental requirements
- Flow requirements for LAT Instrument Performance, Functional & Environmental test
- Track level of verification: Components, Subassemblies, & Subsystem
- Identify method of verification: Test, Analysis, Inspection, & Similarity

### ☐ Performance Verification Matrix

- Easily track and verify each ACD requirement
- Details each requirement's verification level, method and origin



# ACD Test Requirements

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## Electrical

### Electrical Interface

- Isolation /Continuity Checks
- Open Circuit Voltage Checks
- Initial Power Turn-On

### Aliveness

### Limited Functional

### Full Functional

### Comprehensive Performance

## Mechanical

### Static Load

### Sine Sweep Vibration (Modal Survey)

### Sine Vibration, 3 Axis

### Random Vibration

### Acoustic

### Mass Properties

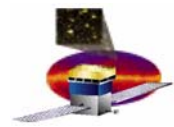
## Environmental

### Thermal Vacuum

### Thermal Balance

### EMI/EMC

**ACD-PLAN-000050–D5, LAT ACD Subsystem - ACD Verification Plan**



# ACD Environmental Testing

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**Environmental Testing already performed on Qualification Subassemblies, consisting of shell section, flexures, tiles, waveshifting fibers, optical connector, clear fibers, and photomultiplier tubes with resistor network in housing:**

- **ACD-PLAN-000032, LAT-ACD Tile Detector Test Vibration Test Plan**
- **ACD-PROC-000068, TDA-PMT-Resistor Network End-to-End Thermal-Vacuum Test Procedure**

**Functional testing for these environmental tests used these procedures:**

- **Tile Detector Assembly (TDA) Test B Procedure**
- **Tile Detector Assembly (TDA) Test A Procedure**

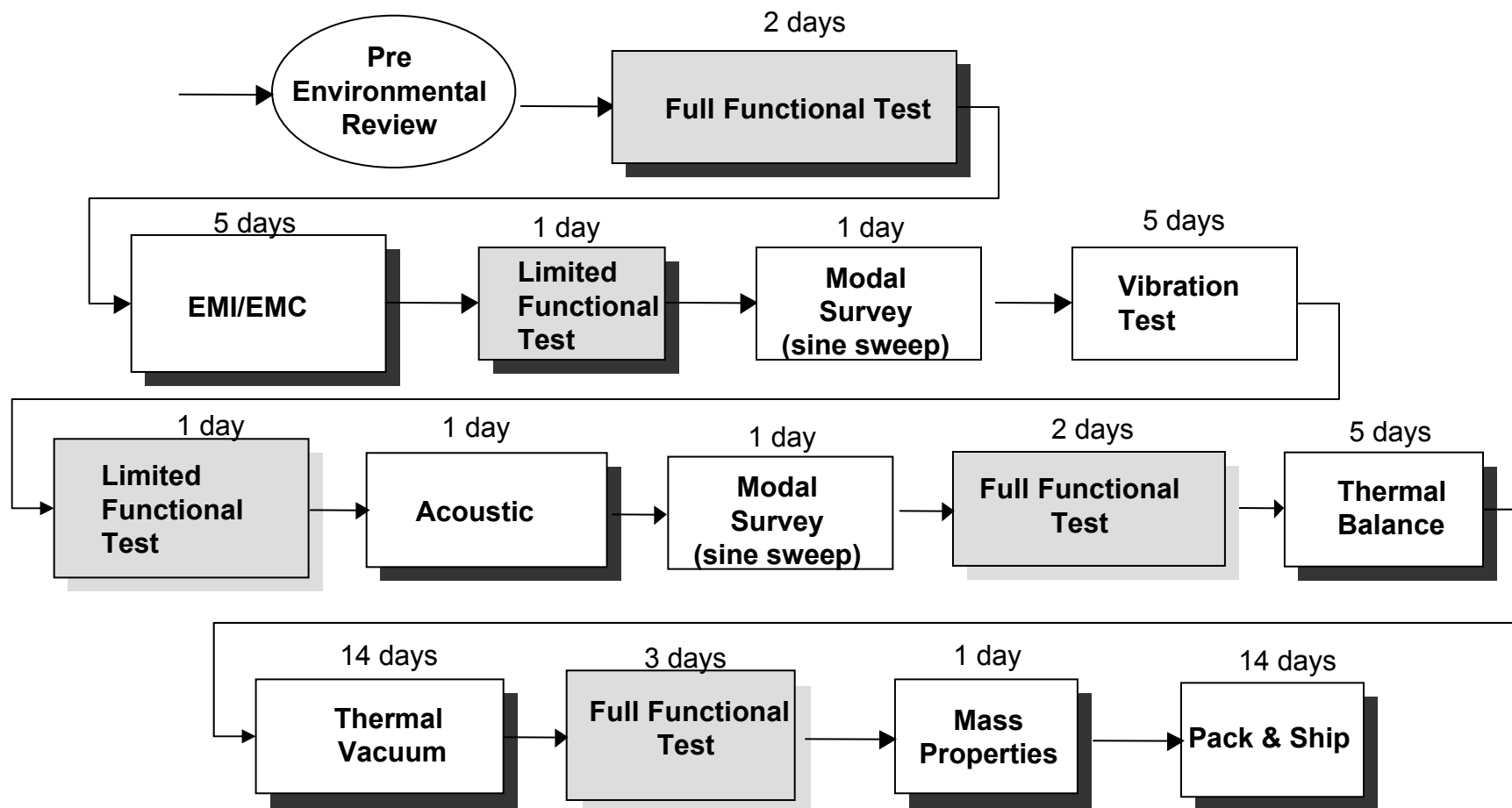
**Experience gained with these tests is being used to write the full ACD Environmental Test procedures**

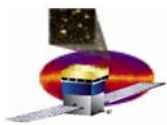
**All Environmental Testing will be carried out in Goddard testing facilities used for many previous instruments and spacecraft.**



# Environmental Test Flow

- Setup test outlines are consistent with 568-PG-8700.1.1 Rev A





# Performance Tests

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## LAT-TD-01112-D1, ACD Functional Test Plans (Comprehensive Performance Test)

### ☐ Aliveness Test (AT)

Functional test that turns on the ACD in a nominal state and verifies basic operation of all channels

### ☐ Functional Tests

- Limited Functional Test (LFT) - Test all major functions of the ACD system
- Full Functional Test (FFT) - Test all functions of the ACD system except a complete measurement of all the ACD tile efficiencies

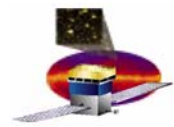
### ☐ Comprehensive Performance Test (CPT)

Test all functions of the ACD system and includes a complete measurement of all the ACD tile efficiencies. Requires rotation of ACD into three different orientations.

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- ```
graph TD; QAO[Quality Assurance Office] --> ACD_I_T[ACD I&T Lead]; QAO --> ACD_SM[ACD Subsystem Manager]; ACD_I_T <--> ACD_SM; ACD_I_T <--> ACD_LE[ACD Lead Engineers]; ACD_I_T <--> ACD_SE[ACD System Engineer]; ACD_I_T <--> ACD_SC[ACD Scientist]; ACD_SM <--> LAT_IS[LAT Instrument Scientists]; ACD_SM <--> LAT_SL[LAT System Leads]; LAT_IS -.-> ACD_SC; subgraph LAT_Box [ ]; LAT_PM[LAT Project Manager]; end
```
- The diagram illustrates the organizational structure of the Quality Assurance Office. At the top is the **Quality Assurance Office** (orange box). Below it are two main branches: **ACD I&T Lead** (yellow box) and **ACD Subsystem Manager** (yellow box). The **ACD I&T Lead** is connected to **ACD System Engineer** (purple box), **ACD Lead Engineers** (purple box), and **ACD Scientist** (purple box). The **ACD Subsystem Manager** is connected to **LAT Instrument Scientists** (green box) and **LAT System Leads** (green box). A dashed line connects **LAT Instrument Scientists** to **ACD Scientist**. A **LAT Project Manager** (green box) is also shown within the LAT group.

Higher level anomalies that are affecting Science, Lat instrument or other subsystems will be flowed up to the LAT Project System Leads & LAT Instrument Scientists for resolution, then back through ACD Subsystem Manager to ACD I&T Lead for implementation

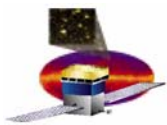




# Key I&T Schedule

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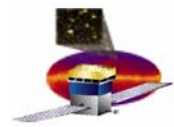
|                                            |           |    |
|--------------------------------------------|-----------|----|
| ▪ Flight Hardware starts to arrive for I&T | September | 03 |
| ▪ TSA assembly complete                    | December  | 03 |
| ▪ BEA assembly complete                    | March     | 04 |
| ▪ ACD Integration Complete                 | March     | 04 |
| ▪ Environmental Test Starts                | May       | 04 |
| ▪ Ship ACD to SLAC                         | Aug       | 04 |



# Issues/Concerns

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- **Need commitment from Goddard for Test Conductor support**
- **Readiness of LAT Test Stand delivery to support ACD I&T (ACD/LAT Electronics – Testing Interface Document, LAT-TD-01205, Draft)**



# Summary

| <b>ACD Element</b>              | <b>Progress to Date</b>                                                                                       | <b>Status</b>                                                                            |
|---------------------------------|---------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|
| <b>MGSE</b>                     | <b>Modifying existing hardware</b>                                                                            | <b>Will be ready when needed</b>                                                         |
| <b>EGSE test scripts</b>        | <b>Scripts outlined, GARC test script written.</b>                                                            | <b>Partially dependent on new interface hardware from LAT Electronics, due in April.</b> |
| <b>Assembly plan</b>            | <b>Detailed outline</b>                                                                                       | <b>Will be ready when needed.</b>                                                        |
| <b>Functional testing plans</b> | <b>Functional tests for phototubes and tile detectors ready.<br/>Comprehensive Performance Test in review</b> | <b>Building larger tests from individual component tests already completed.</b>          |
| <b>Verification plans</b>       | <b>Verification plan in signoff;<br/>Environmental tests in draft</b>                                         | <b>Building larger tests from subassembly tests.</b>                                     |